CLAIMS:

1. A buffer circuit (31) for a signal wire of an integrated circuit in which one or more aggressor signals can have a degrading effect on the signal wire, the buffer circuit (31) receiving an input signal and producing an output signal, and comprising first and second inverter stages (7, 9), characterized in that the buffer circuit (31) comprises means (19, 21, 23, 25, 27, 29) for dynamically controlling the switching threshold of the first inverting stage (7) according to the state of one or more of the aggressor signals.

2. A buffer circuit (31) as claimed in claim 1, wherein the means (19, 21, 23, 25, 27, 29) for dynamically controlling the switching threshold receives first and second aggressor signals for controlling the switching threshold.

3. A buffer circuit (31) as claimed in claim 2, wherein the means (19, 21, 23, 25, 27, 29) for dynamically controlling the switching threshold comprises means for lowering the switching threshold when the signal wire is at a first logic level, and the first and second aggressor signals are at a second logic level.

4. A buffer circuit (31) as claimed in claim 3, wherein the switching threshold is lowered by lowering the switching voltage of the first inverting stage (7) when the signal wire is at a low logic level.

5. A buffer circuit (31) as claimed in claim 3, wherein the switching threshold is lowered by raising the switching voltage of the first inverting stage (7) when the signal wire is at a high logic level.

6. A buffer circuit (31) as claimed in claim 2, wherein the means (19, 21, 23, 25, 27, 29) for dynamically controlling the switching threshold comprises means for raising the switching threshold when the signal wire and the first and second aggressor signals are at the same logic level.

7. A buffer circuit (31) as claimed in claim 2, wherein the switching threshold is dynamically controlled for a predetermined period of time, using first and second aggressor signals which are delayed versions of the aggressor signals received from corresponding aggressor signal wires.

8. A buffer circuit (31) as claimed in claim 1, wherein the means (19, 21, 23, 25, 27, 29) for dynamically controlling the switching threshold comprises means for selectively controlling a pull up path and/or a pull down path in the first inverter stage (7).

9. A buffer circuit (31) as claimed in claim 3, wherein the means for lowering the switching threshold comprises:

- additional circuitry connected in parallel to the first inverter stage (7), the additional circuitry receiving first and second control signals (X, Y) for selectively controlling the respective pull up path and pull down path of the first inverter stage (7).

10. A buffer circuit (31) as claimed in claim 9, wherein the additional circuitry comprises:

- first and second p-mos devices connected in parallel to the pull up path of the first inverting stage (7), the first p-mos device having a source connected to a supply voltage (Vdd) and a drain connected to a second p-mos device, the gate of p-mos device being controlled by the input signal, and the gate of the second p-mos device being controlled by the first control signal (X), the drain of the second p-mos device connected to the output of the first inverter stage (7);
- first and second n-mos devices connected in parallel to the pull down path of the first inverting stage (7), the first n-mos device having a drain connected to the output of the first inverting stage (7) and a source connected to the drain of the second n-mos device, the gate of the first n-mos device being controlled by the second control signal (Y), and the gate of the second n-mos device receiving the input signal, and the source of the second n-mos device being connected to ground (gnd).

11. A buffer circuit (31) as claimed in claim 10, further comprising selection logic for providing the control signals (X, Y) according to the following equations:

$$X = \overline{Vin} \cdot Agg1 \cdot Agg2$$

$$Y = \overline{Vin} + Agg1 + Agg2$$

where Vin is the input signal, and Agg1 and Agg2 are the first and second aggressor signals, respectively.

12. A buffer circuit (31) as claimed in claim 11, whereby the selection logic is implemented to meet the following delay criteria:

$$T_{CLK} > T_{SI} > \delta_{max}$$

where, T_{CLK} is the clock period, T_{SI} is the delay of selection logic circuit, δ_{max} is the maximum difference between the delay of the signal input and the aggressor signals.

13. An integrated circuit having an on-chip bus, wherein one or more signal wires in the on-chip bus include a repeater or receiver circuit having a buffer circuit (31) as defined in claim 1.

14. An integrated circuit as claimed in claim 13, having repeater circuits (31) connected in a point-to-point arrangement.

15. A method of buffering a signal on a signal wire of an integrated circuit in which one or more aggressor signals can have a degrading effect on the signal, the method comprising the step of receiving an input signal and producing an output signal using first and second inverter stages (7,9) , the method being characterized by the step of dynamically controlling the switching threshold of the first inverting stage (7) according to the state of one or more of the aggressor signals.